

# Characterization and Modeling of Multiple Coupled On-Chip Interconnects on Silicon Substrate

Ji Zheng, *Member, IEEE*, Vijai K. Tripathi, *Fellow, IEEE*, and Andreas Weisshaar, *Senior Member, IEEE*

**Abstract**—A quasi-magnetostatic integral formulation approach is applied to compute the frequency-dependent series resistance and inductance parameters for coupled microstrip on-chip interconnects on silicon. The method is based on the simultaneous discretization of interconnect conductors and silicon substrate, and takes into account the substrate skin effect (eddy currents), as well as the conductor skin and proximity effects. An efficient equivalent-circuit model based on “effective substrate current loops” is extracted from the frequency-dependent  $R$  and  $L$  parameters for a class of coupled microstrip-type on-chip interconnects. The frequency response of the proposed model consisting of only passive  $R$ ,  $L$  elements agrees well with the broad-band characteristics of the distributed resistance and inductance parameters of the interconnect obtained by electromagnetic simulation. Model extraction results are presented for asymmetric coupled interconnects to demonstrate the proposed method.

**Index Terms**—Eddy currents, equivalent-circuit model, MIS microstrip, on-chip interconnects, quasi-magnetostatic approach, skin effect.

## I. INTRODUCTION

**M**IXED-SIGNAL integrated circuits have been demonstrated to provide high-performance system solutions for various applications such as wireless communications and high-speed communication backbones. The continued scaling and improvement of semiconductor processes have made it possible to integrate RF, analog, and digital circuitry on a common silicon substrate and create system-on-a-chip (SoC) solutions for various mixed-signal applications. Furthermore, RF and microwave integrated circuits in silicon-based CMOS technology are increasingly desirable due to the fabrication cost advantage. However, unlike microwave/RF integrated circuits on low-loss substrates, such as alumina and Si-GaAs, the lossy nature of the semiconducting silicon substrate may have a significant impact on the loss and dispersion characteristics of on-chip interconnects as well as on-chip-wiring-based integrated passive components, such as spiral inductors, in RF, high-speed analog, and mixed-signal integrated circuits. In addition to the substrate loss, the conductor skin and proximity

effects between closely adjacent lines may also contribute to the overall signal dispersion on on-chip interconnects in the form of frequency-dependent series resistance and inductance parameters.

The broad-band transmission-line behavior of interconnects on lossy silicon substrate (typically referred to as metal–insulator–semiconductor (MIS) transmission lines) has been characterized by experiment (e.g., [1]–[3]), by rigorous analytical methods, and by various numerical approaches (e.g., [4]–[7]). In this paper, a general quasi-magnetostatic solver based on an integral formulation [8] is adopted to compute the frequency-dependent distributed resistance and inductance parameters. The proposed method includes the important physical effects (substrate skin effect, conductor skin and proximity effects) associated with on-chip interconnects on lossy silicon. The integral formulation and its corresponding equivalent-circuit interpretation are similar to the well-known partial-element equivalent-circuit approach (PEEC) [9], which has been widely used for characterization of nonuniform packaging structures and passive components. Here, the integral formulation approach is applied to solve for the per-unit-length (p.u.l.) impedance parameters of interconnects placed on a semiconducting silicon substrate.

Equivalent-circuit models for interconnects generally are desirable for circuit designers to incorporate the interconnect structures as a subcircuit into generic circuit solvers, and are of special advantage in co-simulation with nonlinear devices. Frequency-dependent off-chip lossy interconnects have been modeled, for example, by a network consisting of uncoupled lossless transmission lines and synthesized lumped-element subnetworks based on a normal-mode decomposition approach [10]. In this paper, a new and simple computer-aided-design (CAD)-oriented equivalent-circuit model is presented for multiple coupled microstrip on-chip interconnects on lossy silicon substrate. It will be demonstrated by electromagnetic (EM) simulation that for a class of typical microstrip interconnects on lossy silicon with relatively small conductor cross sections, the frequency-dependent behavior of the p.u.l. resistance and inductance parameters may be dominated by the substrate skin effect. The proposed compact equivalent-circuit model for the distributed p.u.l. resistance and inductance parameters is based on “effective substrate current loops,” which are common to all interconnect conductors and consist of only ideal lumped elements. A rigorous extraction procedure is developed to determine the equivalent-circuit parameters. A corresponding compact equivalent-circuit model for the frequency-dependent p.u.l. shunt admittance parameters of coupled interconnects consisting of ideal  $R$  and  $C$  elements has been shown in [7].

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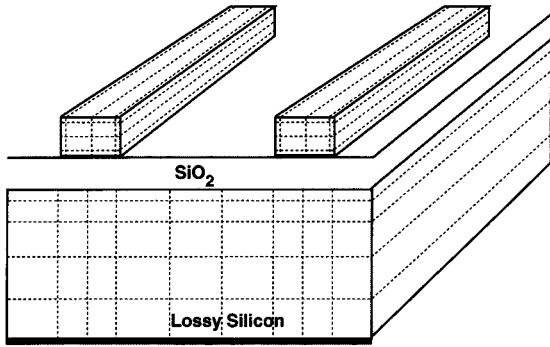


Fig. 1. Discretization of conductors and silicon substrate into filaments of rectangular cross sections to model the frequency-dependent longitudinal current distribution.

## II. QUASI-MAGNETOSTATIC CHARACTERIZATION OF ON-CHIP INTERCONNECTS

To determine the frequency-dependent resistance and inductance parameters p.u.l. of interconnects on lossy silicon, a quasi-magnetostatic integral formulation [8] is applied. Under the quasi-magnetostatic assumption, the current in each interconnect conductor of relatively small cross section can be assumed to flow parallel to its surface. Accordingly, the resulting “eddy currents” in the lossy silicon substrate flow parallel to the conductors. The integral formulation [9] is given by

$$\frac{\vec{J}(r)}{\sigma} + \frac{j\omega\mu}{4\pi} \int_{v'} \frac{\vec{J}(r')}{|r - r'|} dv' = -\nabla\Phi(r) \quad (1)$$

where  $\sigma$  is the conductivity,  $\vec{J}(r)$  is the current density, and  $\Phi(r)$  is the scalar electric potential.

In order to model the frequency-dependent nonuniform longitudinal current distributions in the semiconducting substrate and signal conductors, the substrate, as well as the conductors, are discretized into bundles of volume filaments, as illustrated in Fig. 1. Each filament carries a constant current density along its length and over its cross section. The unknown current distribution can be expressed as

$$\vec{J}(r) = \sum_{i=1}^N \frac{I_i}{a_i} \delta_i(r) \vec{l}_i \quad (2)$$

where  $I_i$  is the current inside filament  $i$ ,  $\vec{l}_i$  is a unit vector along the length of the filament,  $\delta_i(r)$  has a value of zero outside filament  $i$  and one inside, and  $a_i$  is the cross-sectional area. Substituting the current expression into (1) and following the standard procedure in the method of moments with pulse basis functions and point matching, the following matrix equation is obtained:

$$(\mathbf{R} + j\omega\mathbf{L})\mathbf{I}_f = \Phi_f. \quad (3)$$

Here,  $\mathbf{R}$  is a diagonal matrix of filament dc resistances,  $\mathbf{L}$  is a full inductance matrix,  $\mathbf{I}_f$  is a vector of filament currents, and  $\Phi_f$  is a vector of voltage drops across each filament.

The matrix equation can be interpreted in terms of the circuit representation shown in Fig. 2. Each filament is modeled by a series connection of a lumped resistance and inductance. The lumped resistance  $R_i = 1/(\sigma a_i)$  represents the dc resistance of

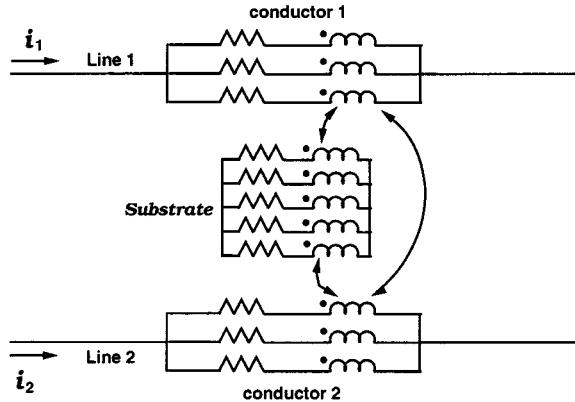


Fig. 2. Equivalent-circuit formulation for distributed series impedance parameters of coupled interconnects on silicon based on (3).

the  $i$ th filament of unit length with cross-sectional area  $a_i$ , and  $\sigma$  is the conductivity of the conductor or the silicon substrate, respectively. Each inductance element represents the inductance of an individual filament of unit length *in the presence of the ground plane*. Furthermore, mutual inductance exists between any two filament-ground loops of unit length in the equivalent circuits and represents the corresponding p.u.l. mutual inductance. These inductance entries, i.e., the p.u.l. self inductance of a filament with rectangular cross section over a ground plane, as well as the p.u.l. mutual inductance of two filaments with rectangular cross sections over a ground plane, can be obtained by extrapolating the corresponding inductance value  $L(l)$  for finite length conductors, as described in the following:

$$L_{\text{p.u.l.}} = \lim_{l \rightarrow \infty} \frac{L(l)}{l}. \quad (4)$$

The self and mutual inductances of finite-length filaments over a ground plane are efficiently obtained from the closed-form expressions for *partial* self and mutual inductance of thin conductors given, for example, in [11] with the aid of appropriate image conductors. It should be noted that *p.u.l. partial* inductance does not exist by the nature of its definition. However, the p.u.l. self and mutual inductance of filaments *in the presence of the ground plane* is convergent when the length is chosen to be sufficiently large. Numerical experiments have shown that a length of 10 000 times the corresponding cross-sectional dimensions is sufficient to guarantee convergence of (4). The convergence behavior of p.u.l. self and mutual inductances is demonstrated in Fig. 3(a) and (b), respectively.

The overall frequency-dependent p.u.l. resistance and inductance parameters are determined by solving for the open-circuit impedance parameters of the equivalent-circuit network [8]. Since the quasi-magnetostatic formulation is based on volume filaments, it is able to handle silicon substrates with nonuniform doping profile. Enhancements in computational efficiency for this approach may be facilitated, for example, by using nonuniform discretization of the silicon substrate and surface-impedance-based methods [12]. The EM simulation results are further compared to the results obtained with the full-wave planar EM field solver Agilent Momentum.<sup>1</sup> The

<sup>1</sup>Agilent EEs of EDA, Santa Rosa, CA.

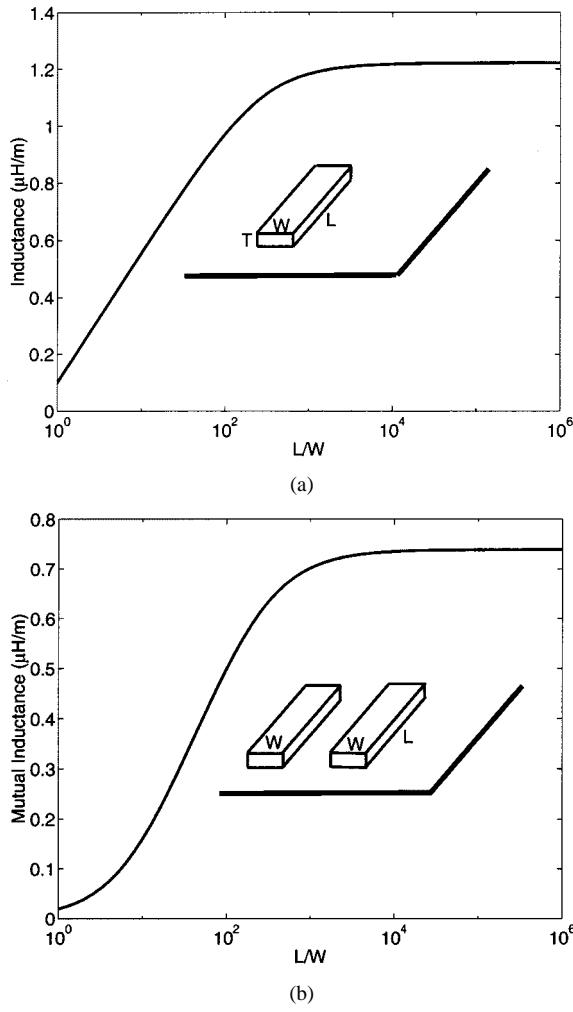


Fig. 3. Convergence of p.u.l. inductance of filaments over a ground plane. (a) Self inductance. (b) Mutual inductance.

comparison is shown in Fig. 4. In this case, the width of the conductors is 20 and 8  $\mu\text{m}$ , respectively, and the spacing between the two conductors is 10  $\mu\text{m}$ . The interconnects are on a 300- $\mu\text{m}$  silicon substrate (resistivity  $\rho_{si} = 0.01 \Omega \cdot \text{cm}$ ) with a 2- $\mu\text{m}$  oxide layer. To demonstrate the validity of the proposed method in handling the lossy substrate, the conductors are chosen to have zero resistivity and thickness. Since the conductor width does not significantly affect the resistance contribution from the lossy substrate, the curves for the two self resistances  $R_{11}$  and  $R_{22}$  in Fig. 4(a) are indistinguishable. The p.u.l. parameters have also been extracted from the four-port scattering parameters obtained with Agilent Momentum. The comparison in Fig. 4(a) and (b) shows good agreement up to 10 GHz between the quasi-magnetostatic and full-wave solutions.

### III. EQUIVALENT-CIRCUIT MODELING

In this section, a simple equivalent-circuit model for coupled on-chip interconnects is developed. Under the quasi-TEM assumption, the frequency-dependent series impedance and shunt admittance parameters of coupled interconnects are modeled separately in terms of ideal lumped equivalent circuits. Here,

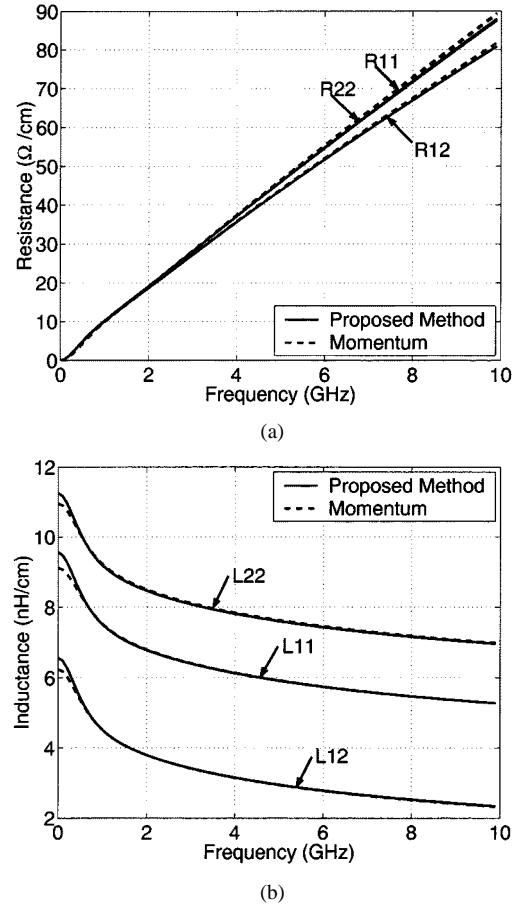
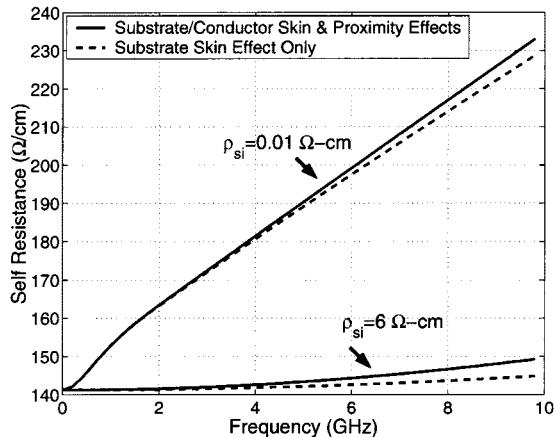


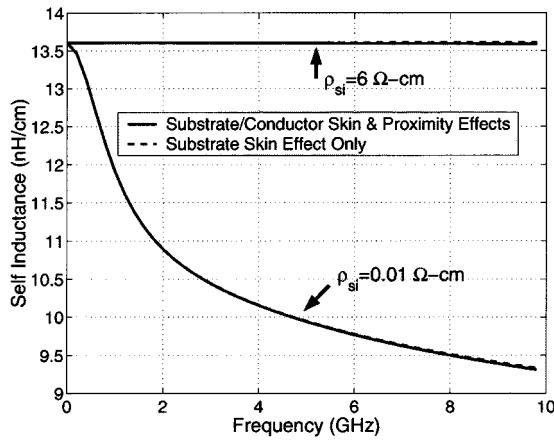
Fig. 4. Comparison of simulation results obtained by the proposed quasi-magnetostatic solver and the planar full-wave solver Momentum for self and mutual p.u.l. impedance parameters of an asymmetric coupled interconnect structure on lossy silicon substrate with resistivity  $\rho_{si} = 0.01 \Omega \cdot \text{cm}$ . (a) Resistance. (b) Inductance. The curves for the two self resistance parameters  $R_{11}$  and  $R_{22}$  are indistinguishable.

the focus is on the development of a compact ideal equivalent-circuit model for the frequency-dependent self and mutual series impedance parameters of coupled on-chip interconnects. A compact equivalent-circuit model for the frequency-dependent p.u.l. shunt admittance parameters has been shown in [7].

The PEEC-like EM solver described in the previous section is used to simulate the frequency-dependent resistance and inductance parameters, which include substrate skin effect, as well as conductor skin and proximity effects. For the most general coupled on-chip interconnects, when both conductor skin/proximity effects and substrate skin effect are significant, the equivalent-circuit model for the series impedance parameters can be obtained via a Cauer- or Foster-type lumped  $R$ ,  $L$  circuit synthesis for the p.u.l. self and mutual impedance parameters. The frequency-dependent inductive and resistive coupling between any two interconnects are then modeled by a set of ideal current-controlled current sources (CCCSs) and voltage-controlled voltage sources (VCVSs), as presented in [7] and [13]. This modeling scheme is based on a rigorous mathematical synthesis of the telegrapher's equations and can be applied to multiple coupled interconnects with general frequency-dependent resistance and inductance parameters. However, the complexity of the equivalent circuit increases exponentially with the number



(a)

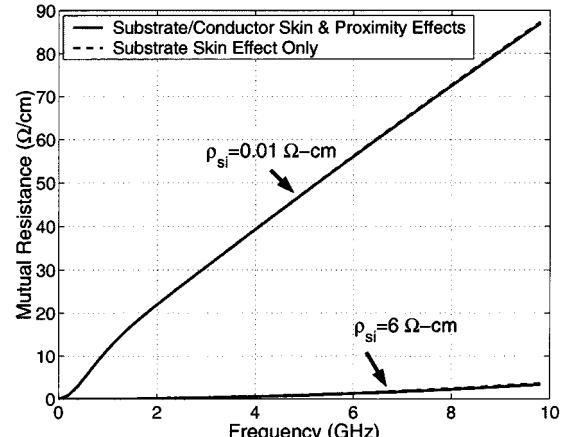


(b)

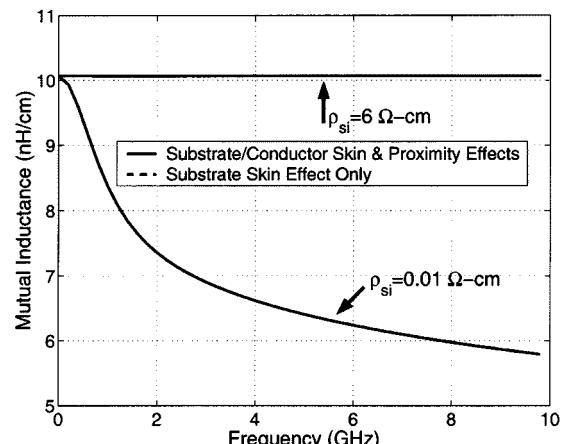
Fig. 5. Self impedance parameters for symmetric coupled interconnects on low- and high-resistivity silicon substrates. (a) Self resistance. (b) Self inductance.

of interconnects. For example, to model a p.u.l. section of three coupled interconnects, nine self and mutual impedance elements need to be synthesized and 12 linear controlled sources need to be employed to represent the mutual coupling among the interconnect conductors. The large number of interconnected controlled sources, however, may cause stability problems in some circuit simulators.

A simpler yet accurate equivalent-circuit model can be obtained by first exploring the relative importance of conductor skin effect and substrate skin effect for a class of on-chip interconnects. The lossy silicon substrate is expected to have a significant impact on microstrip-type interconnects due to the distribution and variation of the magnetic field between the signal conductors and ground plane. Figs. 5 and 6 show the self and mutual resistance and inductance parameters for a coupled on-chip interconnect structure on a low resistivity ( $0.01 \Omega \cdot \text{cm}$ ) and a medium-resistivity ( $6.0 \Omega \cdot \text{cm}$ ) silicon substrate of  $300\text{-}\mu\text{m}$  thickness. The cross section of each conductor is  $2 \mu\text{m} \times 1 \mu\text{m}$  and the separation between the conductors is  $2 \mu\text{m}$ . It can be observed that, in the low-resistivity case, the substrate skin effect is dominant in the frequency dependence of all self and mutual resistance and inductance parameters. In the case of medium substrate resistivity, however, the substrate skin effect is seen to be negligible. This behavior can be explained



(a)



(b)

Fig. 6. Mutual impedance parameters for symmetric coupled interconnects on low- and high-resistivity silicon substrates. (a) Mutual resistance. (b) Mutual inductance.

by considering the skin depth in the conductive substrate. The skin depth in the silicon substrate with conductivity  $\sigma = 1/\rho_{si}$  is given by

$$\delta = \frac{1}{\sqrt{\pi f \mu_0 \sigma}}. \quad (5)$$

Fig. 7 illustrates the relative skin depth in the silicon substrate for medium and low resistivities as a function of frequency. Also shown for comparison is the skin depth in an  $Al$  interconnect conductor. It can be seen that for frequencies above approximately 1 GHz, the skin depth in the low-resistivity substrate is much less than the thickness of the bulk silicon. The large reduction in skin depth to values much less than the substrate thickness results in a significant variation in current density and current distribution in the substrate and, hence, large variations in interconnect resistance and inductance over the 10-GHz frequency range. In contrast, the skin depth in a substrate with medium resistivity remains much larger than the substrate thickness over the entire 10-GHz frequency range.

As a result, a simple CAD-oriented equivalent-circuit model for coupled microstrip on-chip interconnects on silicon has been developed, and is shown in Fig. 8. The new  $R, L$  equivalent

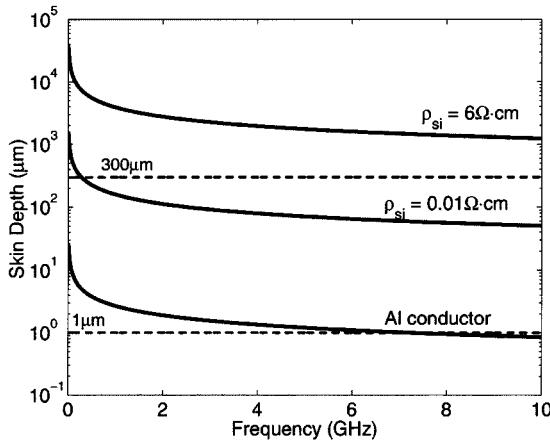
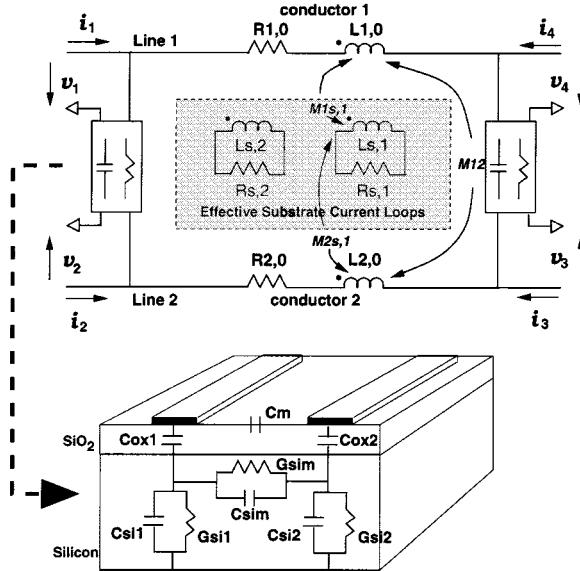
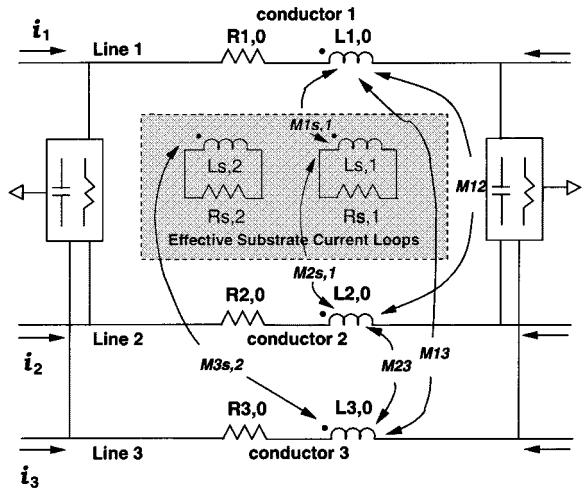


Fig. 7. Skin depth in conductor and silicon substrate as a function of frequency.

Fig. 8. Equivalent-circuit model for coupled on-chip interconnects using two effective substrate current loops. The shunt admittance is modeled in terms of  $R$ ,  $C$  lumped circuits, as shown in [7].

circuit for the series impedance is connected in a  $\pi$ -network configuration with the equivalent-circuit model for the shunt admittance of coupled interconnects consisting of  $R$ ,  $C$  elements [7]. In the proposed model, each interconnect conductor is represented by a series connection of constant resistance and inductance, which correspond to the values of the interconnect dc resistance and inductance in the low-frequency limit. The effects of eddy currents in the substrate (substrate skin effect) are modeled by “effective substrate current loops,” each of which consists of an effective substrate inductance  $L_{s,i}$  and effective substrate resistance  $R_{s,i}$ . The inductive and resistive coupling through the substrate is modeled by constant mutual inductance between each substrate loop and each conductor, in addition to the constant mutual inductance between the conductors. Typically, only up to 3–4 substrate loops are sufficient to accurately model the frequency dependence over a large range of substrate resistivities.

Fig. 9. Equivalent-circuit model for three coupled on-chip interconnects using two effective substrate current loops. The shunt admittance is modeled in terms of  $R$ ,  $C$  lumped circuits, similar to the coupled interconnects shown in Fig. 8.

The equivalent-circuit model for coupled interconnects can be extended to multiple coupled on-chip interconnects with only a minimum increase in complexity by using the same substrate current loop circuit topology to represent the eddy currents in the silicon substrate. As an example, Fig. 9 illustrates the equivalent-circuit topology for three coupled on-chip interconnects. Here, the  $R$ ,  $L$  equivalent circuit for the series impedance is connected with an extended  $R$ ,  $C$  shunt admittance model in a generalized  $\pi$ -network configuration.

It will be demonstrated in the following that a simple extraction procedure based on rational polynomial approximation can be used to extract the  $R$ ,  $L$  equivalent-circuit parameters from the EM simulation data. Without loss of generality, the model extraction approach is described for a coupled interconnect structure. Assume that the currents in the two interconnect conductors are  $I_1$  and  $I_2$ , respectively. Furthermore, the currents in the effective substrate loops are denoted by  $I_{s,i}$ , where  $i = 1, \dots, N$  and  $N$  is the number of loops. The voltage drops across conductors 1 and 2 are given by

$$V_1 = (R_{1,0} + sL_{1,0})I_1 + sM_{12}I_2 + \sum_{i=1}^N M_{1s,i}I_{s,i} \quad (6)$$

and

$$V_2 = (R_{2,0} + sL_{2,0})I_2 + sM_{12}I_1 + \sum_{i=1}^N M_{2s,i}I_{s,i} \quad (7)$$

respectively, where  $M_{1s,i}$  represents the mutual inductance between conductor 1 and the  $i$ th substrate loop, and  $M_{2s,i}$  represents the mutual inductance between conductor 2 and the  $i$ th substrate loop.

The current in the  $i$ th substrate current loop can be expressed in terms of the currents in the interconnect conductors, i.e.,  $I_1$  and  $I_2$ , by solving the following set of equations:

$$(R_{s,i} + sL_{s,i})I_{s,i} + sM_{1s,i}I_1 + sM_{2s,i}I_2 = 0, \quad i = 1, \dots, N. \quad (8)$$

Substituting the expression of  $I_{s,i}$  into (6) and (7) yields an expression for the series impedance parameters in terms of the equivalent-circuit model parameters. The result is given by

$$z_{11} = R_{1,0} + sL_{1,0} - \sum_{i=1}^N \frac{M_{1s,i}^2 s^2}{R_{s,i} + sL_{s,i}} \quad (9)$$

$$z_{12} = sM_{12} - \sum_{i=1}^N \frac{M_{1s,i} M_{2s,i} s^2}{R_{s,i} + sL_{s,i}} \quad (10)$$

$$z_{22} = R_{2,0} + sL_{2,0} - \sum_{i=1}^N \frac{M_{2s,i}^2 s^2}{R_{s,i} + sL_{s,i}}. \quad (11)$$

In the above equations, the model parameters  $R_{i,0}$ ,  $L_{i,0}$ , and  $M_{12}$  are directly obtained from the low-frequency EM simulation results. The remaining model parameters are then extracted by first constructing rational polynomial approximations for  $(R_{1,0} + sL_{1,0} - z_{11})/s^2$ ,  $(R_{2,0} + sL_{2,0} - z_{22})/s^2$ , and  $(sM_{12} - z_{12})/s^2$ , respectively. The coefficients of the rational polynomials having the general form of

$$F(j\omega) = \frac{A_0 + A_1(j\omega) + A_2(j\omega)^2 + \dots + A_m(j\omega)^m}{1 + B_1(j\omega) + B_2(j\omega)^2 + \dots + B_n(j\omega)^n} \quad (12)$$

are determined using a robust fitting approach similar to [14]. Finally, the self and mutual inductance and resistance values for each substrate loop are determined by performing partial fraction expansions and comparing like coefficients. Note that one parameter for each loop can be arbitrarily chosen.

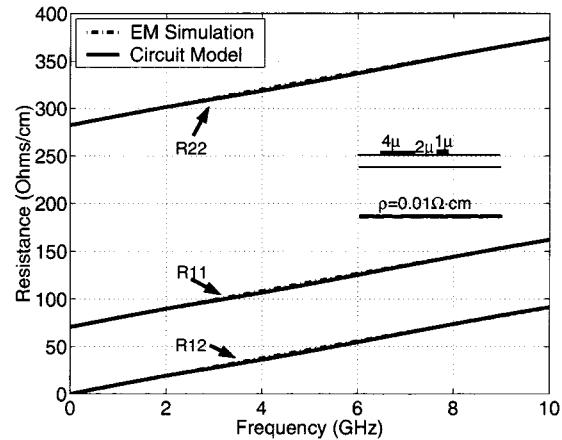
Since the frequency-dependent effects of the lossy substrate are completely represented by the “effective substrate current loops,” which are common to all interconnect conductors, the equivalent-circuit model presented here can be applied to multiple coupled on-chip interconnects without significantly increasing the complexity of the equivalent circuit. In addition, the equivalent-circuit model consists only of passive  $R$ ,  $L(K)$ ,  $C$  lumped elements; hence, it is compatible with the latest passive model reduction techniques such as the passive reduced-order interconnect macromodeling algorithm PRIMA [15]. The use of model order reduction is of special importance for handling longer on-chip interconnect structures. It should be noted further that the equivalent-circuit model presented here may be extended to include the conductor skin effect by constructing additional effective current loops coupled to the individual conductors.

#### IV. MODELING EXAMPLE

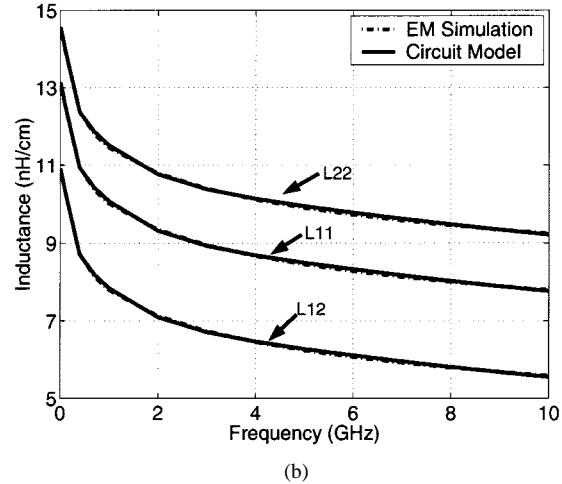
To exemplify the validity and accuracy of the proposed model, the equivalent-circuit parameters are extracted for an asymmetric coupled on-chip interconnect structure. The interconnects are on a silicon substrate of 500- $\mu\text{m}$  thickness (resistivity = 0.01  $\Omega \cdot \text{cm}$ ) with a 2- $\mu\text{m}$  oxide layer. The cross sections of the interconnect conductors are 4  $\mu\text{m} \times 1 \mu\text{m}$  and 1  $\mu\text{m} \times 1 \mu\text{m}$ , respectively. The separation between the two conductors is 2  $\mu\text{m}$ . The frequency-dependent resistance and inductance parameters are obtained by the PEEC-like approach described in the previous section. In this specific case, three effective substrate impedance loops are used. The extracted

TABLE I  
EXTRACTED EQUIVALENT-CIRCUIT PARAMETERS FOR AN ASYMMETRIC COUPLED ON-CHIP INTERCONNECT STRUCTURE ON LOSSY SILICON

Parameters	Extracted value	Parameters	Extracted value
$L_{1,0}$	13.14 nH/cm	$M_{12}$	10.92 nH/cm
$L_{2,0}$	14.58 nH/cm	$M_{1s,1}$	4.806 nH/cm
$R_{1,0}$	70.63 $\Omega/\text{cm}$	$M_{1s,2}$	4.398 nH/cm
$R_{2,0}$	282.5 $\Omega/\text{cm}$	$M_{1s,3}$	4.998 nH/cm
$L_{s,1}$	10.00 nH/cm	$M_{2s,1}$	4.802 nH/cm
$R_{s,1}$	733.9 $\Omega/\text{cm}$	$M_{2s,2}$	4.396 nH/cm
$L_{s,2}$	10.00 nH/cm	$M_{2s,3}$	4.997 nH/cm
$R_{s,2}$	89.39 $\Omega/\text{cm}$		
$L_{s,3}$	10.00 nH/cm		
$R_{s,3}$	11.53 $\Omega/\text{cm}$		



(a)



(b)

Fig. 10. Comparison of simulated and modeled p.u.l.  $R$  and  $L$  parameters for asymmetric coupled on-chip interconnects.

model parameters (lumped  $R$ ,  $L$ , and  $K$  elements) for the interconnects’ series impedance parameters are shown in Table I. The self inductance of the substrate loops has been chosen as  $L_{s,i} = 10 \text{ nH/cm}$  ( $i = 1, 2, 3$ ). The frequency response of the extracted model agrees well with that computed from the EM solution, as shown in Fig. 10.

## V. CONCLUSION

A PEEC-like integral-equation-based EM solver has been applied to characterize the frequency-dependent resistance and inductance parameters for interconnects on lossy silicon. A simplified equivalent-circuit model based on “effective substrate current loops” has been presented for a class of microstrip-type multiple coupled on-chip interconnects, where the substrate skin effect dominates the frequency dependence of distributed line resistance and inductance parameters. The complexity of the equivalent circuit increases only linearly with the number of coupled interconnect conductors since the effect of the lossy silicon substrate has been fully represented by substrate current loops common to all interconnects. Furthermore, the proposed equivalent-circuit model consists of only ideal passive SPICE elements and can be incorporated into generic circuit simulators in terms of a subcircuit. Hence, the new model should be useful in the design of RF and mixed-signal integrated circuits on silicon.

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